Remarks

In the Office Action dated December 14, 2004, the Examiner rejected claims 1-6, 8-11, and 14-21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,065,088 to Bronson et al. ("Bronson") in view of U.S. Patent No. 5,928,354 to Umeki et al. ("Umeki"). Additionally, the Examiner rejected claims 22-25 under 35 U.S.C. § 103(a) over Bronson and objected to claims 7 and 12 as containing allowable subject matter but dependent on a rejected base claim.

By this Amendment, Applicants amend claims 1, 5, 7, 8, 12, 13, and 20 and cancels claims 3, 4, 10, and 11 without prejudice or disclaimer. Claim 1 is amended to include certain features from canceled claims 3 and 4, claim 8 is amended to include certain features from canceled claims 10 and 11, and claim 20 is amended to more appropriately define the invention. Claims 5, 7, and 13 are amended to improve form. Claim 12 is amended to incorporate the previously received features of claims 8 and 11.

In view of the cancellation of claims 3, 4, 10, and 11, Applicants submit that the rejections of these claims are obviated.

Claim 12, as amended, now incorporates the features previously recited in claims 8 and 11. Accordingly, Applicants submit that this claim is allowable over the prior art of record.

As an initial matter, Applicants note that the Examiner did not include claim 13 in the statement of the rejection under 35 U.S.C. § 103(a) in view of Bronson and Umeki, although the Examiner grouped claim 13 in with claims 6

and 18 in the detailed explanation of this rejection. Applicants will assume that the Examiner intended to include claim 13 in the statement of the rejection. Applicants request clarification on the status of this claim.

Rejection under 35 U.S.C. § 103(a)
Based on Bronson and Umeki

Claim 1, as amended, is directed to a queue comprising a first queuing area configured to enqueue and dequeue data, the first queuing area including a plurality of parallel sub-queues that queue a plurality of parallel data. Claim 1 further includes a second queuing area configured to receive data from the first queuing area when the first queuing area has data available to be dequeued. The second queuing area includes a first buffer configured to store a first set of the parallel data and a second buffer configured to store a second set of the parallel data. Claim 1 further recites bypass logic coupled to the second queuing area, the bypass logic configured to bypass the first queuing area and to forward data to the second queuing area when the second queuing area is ready to receive data and the first queuing area is empty.

Applicants submit that Bronson and Umeki, either alone or in combination, fail to disclose or suggest each of the elements recited in claim 1. These references, for instance, fail to disclose or suggest the first and second queuing areas recited in claim 1.

Bronson is directed to systems and methods for interrupt command queuing and ordering. (Bronson, Title). The Examiner contends that interrupt routing unit 142 of Bronson (see Bronson, Fig. 3) corresponds to the claimed first queuing area and the remaining queues correspond to the claimed second

queuing area (Office Action, page 2). Applicants respectfully disagree with the Examiner's interpretation of Bronson.

Interrupt routing unit 142 of Bronson handles interrupt commands and is particularly discussed by Bronson at column 8, lines 20-54. As disclosed by Bronson, interrupt routing unit 142 has two separate command queues, queue 136 for EOI (end-of-interrupt) commands and queue 134 for both INR (interrupt return) and IRR (interrupt reissue request) commands. (Bronson, col. 8, lines 20-23). The EOI commands output from queue 136 are fed into queue 146, which, according to Bronson, is "implemented as a strict First In First Out (FIFO) queue." (Bronson, col. 8, lines 33-36). The INR and IRR commands output from queue 134, on the other hand, are delivered to high priority I/O command queue 150. (Bronson, col. 8, lines 42-45).

Bronson can not be said to include, as recited in claim 1, a first queuing area configured to enqueue and dequeue data, the first queuing area including a plurality of parallel sub-queues that queue a plurality of parallel data. The feature of claim 1 relating a plurality of sub-queues was previously recited in claim 3, which the Examiner rejects based on the contention that EOI output queue 136 and INR/IRR output queue 134 of Bronson correspond to this feature of claim 1. (Office Action, page 4). Applicants respectfully disagree with the Examiner's interpretation of Bronson. Although queues 136 and 134 of Bronson define multiple queues, these queues appear to each be separate queues that are used to queue different commands and that output the commands to different output queues. Accordingly, it is not accurate to interpret these queues as a "plurality of sub-queues" that queue "a plurality of parallel data." Queues 136 and 134 are

not sub-queues of a larger queue, they are independent queues that are part of an interrupt routing unit 142.

Amended claim 1 further recites that the second queuing area includes a first buffer configured to store a first set of parallel data and a second buffer configured to store a second set of the parallel data. This feature was previously recited in now-canceled claim 4. The Examiner contends that this feature is disclosed by priority queues 148 and 150 of Bronson. (Office Action, page 4). Applicants submit that queues 148 and 150 of Bronson are not buffers that store first and second sets of parallel data. Queues 148 and 150 are described by Bronson as a "normal priority queue" that receives commands from command queue 146 and a "high priority queue" that receives commands from output queue 134. Because these queues correspond to different priority data and receive different types of commands from different sources, it is not accurate to say that these queues correspond to first and second buffers of a single queue that store first and second sets of parallel data. Queues 148 and 150 are two independent queues, not buffers of a single queuing area. Additionally, queues 148 and 150 do not store sets of parallel data, instead, the data in queues 148 and 150 appear to progress through queues 148 and 150 in a non-parallel manner in which queue 150 is given higher priority.

Claim 1 further recites bypass logic coupled to the second queuing area, the bypass logic configured to bypass the first queuing area and to forward memory access requests to the second queuing area when the second queuing area is ready to receive memory access requests and the first queuing area is empty. The Examiner concedes that Bronson does not disclose this bypass

logic, but contends that Umeki discloses the recited bypass logic and that one of ordinary skill in the art would have found it obvious to combine Bronson and Umeki to obtain the features recited in claim 1. Applicants respectfully disagree.

Applicants have reviewed Umeki and submit that Umeki does not cure the above-mentioned deficiencies of Bronson. Accordingly, Bronson and Umeki, either alone or in combination, do not disclose all of the features recited in claim 1.

Additionally, Applicants submit that the Examiner has not made a proper *prima facie* case of obviousness, as one of ordinary skill in the art would not combine Bronson and Umeki as the Examiner suggests. More particularly, the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to bypass the first queuing area of Bronson et al. as done by Umeki et al. since doing so improves access reliability and speed." (Office Action, paragraph bridging pages 2 and 3). Umeki discloses skipping an instruction queue buffer 2 leading to a CPU 4. Applicants submit that an instruction queue buffer leading to a CPU is not reasonably related to an interrupt routing unit, such as unit 142 of Bronson. Accordingly, one of ordinary skill in the art reading Umeki would not be motivated to bypass interrupt routing unit 142 of Bronson in the manner suggested by the Examiner.

For at least these reasons, Applicants submit that the rejection of claim 1 under 35 U.S.C. § 103(a) is improper and should be withdrawn. The rejections of claims 2, 5, and 6, at least by virtue of their dependency from claim 1, are also improper and should be withdrawn.

Claims 8 and 11 also stand rejected under 35 U.S.C. § 103(a) based on Bronson and Umeki. Applicants respectfully traverse this rejection.

Claim 8, as amended, is directed to a method of masking latency in a queue. The method includes receiving incoming data items for the queue that include a plurality of data items for each cycle of the queue. The method further includes forwarding the incoming data items to a buffer when the queue is empty and the buffer is free to receive data items, wherein the buffer includes a first buffer and a second buffer, and wherein higher priority data items are stored in the first buffer and lower priority data items are stored in the second buffer. The method further includes enqueuing the incoming data items in the queue when the queue contains data items or the buffer is not free to receive data items, dequeuing data items from the queue to the buffer when the buffer is free to receive data items, and transmitting the data items from the buffer as the output of the queue.

Bronson and Umeki do not disclose or suggest the combination of features recited in amended claim 8. The Examiner contends that Bronson discloses many of the features recited in claim 8 but concedes that Bronson does not disclose forwarding data items to a buffer when a queue is empty. For this, the Examiner relies on Umeki. (Office Action, page 3).

Applicants submit that Bronson and Umeki, alone or in combination, do not disclose or suggest all of the features recited in claim 8. Bronson, for instance, does not disclose or suggest receiving incoming data items for a queue that include a plurality of data items for each cycle of the queue, as recited in claim 1. The Examiner contends that queue 146 of Bronson corresponds to this

queue. (Office Action, page 3). Queue 146, however, is not disclosed as receiving a plurality of data items for each cycle of the queue. Instead, Bronson explicitly discloses using a multiplexer 144 at the input of queue 146 to select between the MMIO commands and the EOI commands. Accordingly, it appears to Applicants that multiplexer 144, if anything, actually teaches away from receiving a plurality of data items for each cycle of the queue, as recited in claim 8. Further, queue 146 of Bronson is graphically illustrated as a linear array of single slots, which further tends to show that queue 146 of Bronson is not capable of receiving "a plurality of data items for each cycle of the queue," as recited in claim 8.

This feature of claim 8 relating to a plurality of data items for each cycle of the queue was originally recited in claim 10. In rejecting claim 10, the Examiner states that Bronson "teaches the queuing to memory mapped input/output (MMIO) commands as well as memory interrupt commands." (Office Action, page 4). As mentioned above, although queue 146 is disclosed as receiving both MMIO commands and interrupt commands, multiplexer 144 arbitrates between these two commands as they enter queue 146. Accordingly, queue 146 does not receive a plurality of data items for each cycle of the queue, as recited in claim 8.

Further, as discussed above, Applicants submit that the Examiner has not made a proper *prima facie* case of for combining Bronson and Umeki as the Examiner suggests. Umeki discloses skipping an instruction queue buffer 2 leading to a CPU 4. An instruction queue buffer leading to a CPU is not reasonably related to the input/output bus bridge and command queuing system

of Bronson. Accordingly, one of ordinary skill in the art reading Umeki would not be motivated to modify Bronson in the manner suggested by the Examiner.

For at least these reasons, Applicants submit that Bronson and Umeki, either alone or in combination, do not disclose or suggest each of the features recited in claim 8. Accordingly, the rejection of this claim is improper and should be withdrawn.

Claim 13, which depends from claim 8, was additionally rejected under 35 U.S.C. § 103(a) in view of Bronson and Umeki. At least by virtue of its dependency from claim 8, Applicants submit that the rejection of this claims is improper and should be withdrawn.

Independent claim 14 and its dependent claims 15-19 also stand rejected under 35 U.S.C. § 103(a) in view of Bronson and Umeki.

Claim 14 is directed to a network device including, among other things, a request manager configured to receive memory requests, a plurality of parallel processors configured to receive the memory requests from the request manager, and a memory request arbiter configured to receive the memory requests from the plurality of processors. The Examiner contends that Bronson discloses or suggests these features of claim 14. In particular, the Examiner appears to concede that Bronson does not disclose a plurality of parallel processors, as recited in claim 14, but contends that Bronson "could be coupled to multiple processors via the system bus 100." Applicants respectfully disagree with the Examiner's interpretation of Bronson.

Bronson discloses an input/output bus bridge and command queuing system. (Bronson, abstract). Nothing in Bronson discloses or suggests that the

bus bridge of Bronson could be coupled to a plurality of parallel processors configured in the manner recited in claim 14. In particular, the plurality of parallel processors recited in claim 14 receive memory requests from the request manager and a memory request arbiter receives the memory requests from the plurality of processors. If I/O bus 102 of Bronson could be connected to multiple parallel processors (a point Applicants do not concede), the parallel processor of Bronson would receive commands from the bus bridge system. This would still not disclose or suggest the network device of claim 1, which receives memory requests from the plurality of processors. The I/O bus bridge system of Bronson would not be configured to receive memory requests from a plurality of parallel processors, as it is specifically disclosed by Bronson as receiving commands from a system bus 100. System bus 100 of Bronson appears to refer to a system bus for a single processor, such as a bus for a PowerPC computer. (Bronson, col. 1, lines 11-13).

Accordingly, Bronson does not disclose or suggest the request manager, the plurality of parallel processors, and the memory request arbiter, as recited in claim 14.

The memory request arbiter of claim 14 is further recited as including: an input port connected to receive the memory requests from the plurality of processors, a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor, and a buffer configured to receive memory requests dequeued from the queues when the queues contain memory requests and to receive memory requests directly from the input port when the queues do

not contain memory requests. Neither Bronson nor Umeki, either alone or in combination, disclose or suggest these features of claim 14.

For example, neither Bronson nor Umeki disclose or suggest "a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor." Because neither Bronson nor Umeki disclose parallel processors, neither Bronson nor Umeki could possibly disclose the corresponding queues recited in claim 14. The Examiner does not appear to specifically address this feature in the Office Action.

Further, Applicants submit that the Examiner has not made a proper *prima facie* case of for combining Bronson and Umeki as the Examiner suggests. Umeki discloses skipping an instruction queue buffer 2 leading to a CPU 4. An instruction queue buffer leading to a CPU is not reasonably related to the input/output bus bridge and command queuing system of Bronson. Accordingly, one of ordinary skill in the art reading Umeki would not be motivated to modify Bronson in the manner suggested by the Examiner.

For at least these reasons, Applicants submit that Bronson and Umeki, either alone or in combination, do not disclose each of the features recited in claim 14. Accordingly, the rejection of claim 14 is improper and should be withdrawn. Claims 15-19 depend from claim 14. At least by virtue of this dependency, Applicants submit that the rejection of these claims is also improper and should be withdrawn.

Independent claim 20 was also rejected by the Examiner under 35 U.S.C. § 103(a) in view of Bronson and Umeki. This claim, as amended, includes

features similar to those recited in claim 8. Accordingly, for reasons similar to those given above with regard to claim 8, Applicants submit that the rejection of claim 20 under 35 U.S.C. § 103(a) is also improper and should be withdrawn.

Rejection under 35 U.S.C. § 103(a)
Based on Bronson

Claim 22 is directed to an arbiter comprising a queue, a multiplexer, and arbitration logic. The queue is configured to enqueue data items at a first stage of a plurality of stages and dequeue the data items at a last stage of the plurality of stages of the queue. The multiplexer has a plurality of inputs connected to different stages of the queue. The multiplexer outputs selected ones of the data items read from the queue. The arbitration logic is coupled to the queue and controls the multiplexer to output the selected ones of the data items by selecting a predetermined number of data items from the queue during an arbitration cycle, the arbitration logic giving higher priority to data items in later stages of the queue.

The Examiner, in rejecting claim 22 contends that Bronson discloses a plurality of queues, but concedes that Bronson does not "teach the use of a multiplexer connected to multiple stages of a queue, outputting selected data items, and coupled to and controlled by the I/O bus control logic 152." (Office Action, paragraph spanning pages 5 and 6). The Examiner, however, contends that this would have been an obvious modification "since multiplexers are shown to be used in the selection of signals (Figure 3, reference #144) and such a component would be useful in selecting signals from either bus 149 or bus 151 (Figure 3)." (Office Action, page 6).

Applicants submit that the Examiner has not made a proper *prima facie* case of obviousness under § 103. Although Bronson does disclose a multiplexer 144, multiplexer 144 is not configured like the multiplexer recited in claim 22. In stark contrast, multiplexer 144 is explicitly shown as connecting only to the input of command queue 146. Bronson is completely devoid of any disclosure or suggestion to modify the multiplexer of Bronson as suggested by the Examiner. The fact that a multiplexer can be used to "select signals" in no way discloses or suggests the multiplexer of claim 22, which "has a plurality of inputs connected to different stages of the queue." Applicants submit that the Examiner, in making the rejection of claim 22, is impermissibly using hindsight gleaned from Applicants' specification.

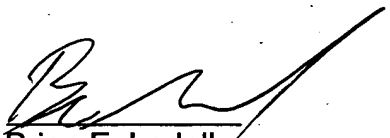
For at least these reasons, Applicants submit that the rejection of claim 22 under § 103 is improper and should be withdrawn. The rejection of claims 23-25, at least by virtue of their dependency on claim 22, is therefore improper and should also be withdrawn.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 CFR 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

By: 
Brian E. Ledell
Reg. No. 42,784

11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800
Customer Number: 44987

Date: March 14, 2005